

[19] Intellectual Property Bureau of the Peoples' Republic of China

[51] Int. Cl⁷
G08B 13/14

[12] Invention Patent Public Announcement

[21] Application No. 99807676.7

[43] Announcement Date: September 26, 2001

[11] Announcement No. CN 1315027A

[22] Date of Application: June 18, 1999 [21] Application No.: 99807676.7

[30] Priority Right:

[32] June 23, 1998 [33] US [31] 09/103,226

[86] International Application: PCT/US99/13645 June 18, 1999

[87] International Publication: WO99/67754 British December 29, 1999

[85] Date Entering National Phase: December 21, 2000

[71] Assignee: Motorola Inc.

Address: Illinois, USA

[72] Inventor: Noel. H. Eberhardt

[74] Patent Representative Agency: Zhong Yuan Xin Da Intellectual Property Representative Co. Ltd.

Representatives: YU Meng, and LI Hui

Patent Claims 2 pages; Descriptions 11 pages; Graphs and Drawings 3 pages

[54] Name of Invention: A Radio Frequency Identification Tag with Printed Antenna and Method

[57] Abstract

A radio frequency identification tag (14) which includes a radio frequency identification tag circuit chip (12); the radio frequency identification tag circuit chip is coupled to an antenna (10) including a conductive pattern (22) printed on a substrate (16). The said substrate may be forming a portion of an article, a package, a package container, an envelope, a certificate, a freight bill, a label and/or an identification badge. The said conductive pattern includes a first coupling area (28) and a second coupling area (30) being designed on or coupled to the radio frequency identification tag circuit chip. The first coupling area and the second coupling area are precisely positioned (located) and separated from one another through a slit (gap) (31) formed on the substrate.

(A cross sectional view of this invention, similar to Figure 9, is shown to the right of the abstract)

Published by Intellectual Property Publisher

ISSN 1008 - 4274

BEST AVAILABLE COPY

Patent Claims

1. A radio frequency identification tag, which is including:

A radio frequency identification tag circuit chip, secured to an antenna, the said antenna is including a first antenna element and a second antenna element forming on the surface of the substrate; the first antenna element and the second antenna element are separated from one another through a slit formed on the substrate.

2. A radio frequency identification tag as in Claim 1, in which the first antenna element is including a first coupling region (area), while the second antenna element is including a second coupling region (area); and the said slit is separating the first coupling region from the second coupling region.

3. A radio frequency identification tag as in Claim 2, in which the first coupling region and the second coupling region are designed to couple with the radio frequency identification tag circuit chip.

4. A radio frequency identification tag as in Claim 1, in which the slit is formed relative to a reference on the substrate.

5. A radio frequency identification tag as in Claim 1, in which the said antenna is a conductive pattern printed on the surface of a substrate.

6. A radio frequency identification tag as in Claim 1, in which a conductive adhesive is used to couple the radio frequency identification tag circuit chip to the said antenna.

7. An antenna for a radio frequency identification tag, which is including:

A conductive pattern that is printed on the surface of a substrate, and a slit that is formed on the substrate, separating the conductive pattern into a first antenna element and a second antenna element.

8. An antenna as in Claim 7, in which the first antenna element is including a first coupling region, and the second antenna element is including a second coupling region; the first coupling region and the second coupling region are defined by the slit.

9. An antenna as in Claim 7, in which the antenna is forming a portion of an article, a package, a package container, an envelope, a certificate, a freight bill, a label and an identification badge.

10. A radio frequency identification tag as in Claim 7, in which the slit is formed relative to a reference on the substrate.

11. A method for preparing a radio frequency identification tag, the said method is consisting of the following steps:

- Providing a substrate with a surface;
- printing a conductive pattern on the said surface;
- forming a slit on the said substrate relative a reference on the substrate; the said slit is separating the conductive pattern into a first antenna element and a second antenna element; and
- connecting a radio frequency identification circuit chip to the first antenna element and the second antenna element.

12. A method as in Claim 11, in which the steps for printing the conductive elements are including printing a first antenna element and a second antenna element which are connected to a first coupling region and a second coupling region, respectively; and a step for forming a slit, including forming the slit that is separating the first coupling region and the second coupling region.

Descriptions

A Radio Frequency Identification Tag with Printed Antenna and Method

This application is submitted on June 9, 1998, by Noel H. Eberhardt, et al, "A Radio Frequency Identification Tag with Product Integrated Antenna", application serial No. _____, representative (attorney) recording No. IND 10149, as a partial continuing application of commonly assigned US patent applications, the earlier applications are cited here as references, the disclosed contents may be similarly described here in the same words and have similar effects.

This application is related to the following earlier commonly assigned US patent applications. Ted Geiszler, et al, submitted on October 11, 1995, application serial No. 08/540831, "Remotely powered electronic tag and associated exciter (driver)/reader and related method", representative recording No. IND00701; Victor Allen Vega, et al, submitted on February 27, 1998, application serial No. 09/031848, "Radio frequency identification tag system using ground coupling connection design", representative recording No. IND10153; Victor Allen Vega, et al, submitted on March 12, 1998, application serial No. 09/041480, "Radio frequency identification tag design for magnetically stored tag state information", representative recording No. IND10153; and Victor Allen Vega, et al, submitted on March 20, 1998, application serial No. 09/045357, "Radio frequency identification tag with programmable circuit state", representative recording No. IND10174; these earlier applications are cited here as reference, the disclosed contents may be similarly described here in the same words and have similar effects.

The invention is generally relating to the field of radio frequency identification tag, including but not limited to radio frequency identification tag with printed antenna.

Radio frequency identification tag and radio frequency identification tag system are known; they have many applications. For example, radio frequency identification tags are often used for personnel identification for guarding an automated gate, to protect the security and safety of a building or an area. Radio frequency identification tag system is used to identify a person whose information is stored in a radio frequency identification tag and is seeking to gain access to a building. Radio frequency identification tag system, use radio frequency (RF) data transmission technology, conveniently provides in a close proximity, to read information from a radio frequency identification tag. Usually, the user simply hand held or place the radio frequency identification tag near a base station, the base station send excitation signal to the supply circuit of the radio frequency identification tag in the radio frequency identification tag. In response to the excitation signal, the said circuit is sending the stored information from the radio frequency identification tag to the base station; the base station then receives and decodes the said information. Usually, radio frequency identification tag can retain and transmit abundant operational information – sufficient information to uniquely identify a person, a package, or inventory, etc.

Typical technology used for supplying power and reading a radio frequency identification tag is inductive coupling, or a combination of inductive power coupling and capacitive data coupling. Inductive coupling is using a coil element in the radio frequency identification tag. The said coil element is excited by an excitation (driver) signal from the base station, providing power to the radio frequency identification tag. The coil in a radio frequency identification tag, or a second coil, may be used to transmit and receive stored information between the radio frequency identification tag and the base station. The radio frequency identification tag is relying on inductive coupling, and the radio frequency identification tag is directional sensitive against the base station; the electric field created by the excited signal must intersect the coil element essentially at a right angle for effective coupling. The reading range of inductive coupling device, in general, is in the order of millimeters. For certain applications, such as electronic pet animal identification, baggage tracking, parcel tracking, and inventory management application, a longer reading distance is needed.

Another technology, used for radio frequency identification tag power supply and reading, is electro static coupling; for example, those disclosed in the references cited above and used for radio frequency identification systems and radio frequency identification tags. These systems beneficially provide visible increases in reading/writing distances for those applications using current technology. Another advantage from the disclosed systems and tags is that the user does not require to place the radio frequency identification tag near the base station or in the direction of the base station. Therefore, it is possible to incorporate the antenna of the base station with, for example, a system in a door, lobby, parcel transporting equipment, or an article sorting system, to supply power to or reading information from the tag at a greater distance.

In order to couple inductive or electrostatic signals between the base station and the radio frequency identification tag, the tag must include an antenna, with at least one, but usually two antenna elements. Usually, the tag circuit chip and antenna are electrically connected and attached to a tag substrate. The tag dimension which is determined by the tag substrate dimension is usually maintained very small. Therefore, the size of antenna of antenna is usually being limited. However, a smaller antenna is adversely affecting the reading range. The antenna also must be formed in the same plane with the tag substrate, which latently making the tag directional sensitive. Because it is not desirable, nor practical, to make the radio frequency identification tag much bigger, the effective antenna size remains being restricted. The usual planar tag design is also limiting the antenna to be in a planar, directionally sensitive configuration.

According to a preferred application example in an above mentioned US patent entitled "Radio frequency identification tag with an article integrated antenna", it is proposing that the antenna is being integrated with an article. For example, in a preferred application example, the antenna is being printed on a card or a packaging paper with a conductive ink; then the radio frequency identification tag chip is secured on the article and is connected to the antenna. In addition, it is proposing to provide a radio frequency identification tag chip assembly. The said chip assembly is providing to bond the radio frequency identification tag circuit chip to a substrate with conductive pattern. As is being disclosed, a

preferred conductive pattern is being formed on a paper substrate through printing with a conductive ink; then the said chip assembly is secured to the article and connected to the said antenna through the conductive pattern.

As is understood, the alignment of the circuit chip with the antenna printed on an article or with the conductive pattern printed on the substrate is very important for proper functioning of the said circuit chip. More specifically, the circuit chip must be positioned within approximately ± 0.125 mm, in order to properly matching the conductive soldering pads with the said antenna and/or the conductive pattern. However, the usual technology for printing antenna and/or conductive pattern on a paper or paper like material has an edge tolerance in the order of ± 1.5 mm. The size of the edge tolerance is larger than a typical circuit chip. The factors for producing imprecise edge tolerance include edge bleeding of the printed pattern and change of printed pattern relative to the substrate location.

Therefore, an improved radio frequency identification tag is needed.

The preferred demonstrative application examples of this invention are explained in the attached figures. Similar reference numbers are representing similar components in the figures.

Figure 1 is an exploded assembly view of a preferred example of a radio frequency identification tag of this invention.

Figure 2 is a cross sectional view along the 2-2 line of Figure 1.

Figure 3 is a planar view of an antenna and/or conductive pattern printed on a substrate.

Figure 4 is an enlarged planar view of the antenna portion in Circle A of Figure 3.

Figure 5 is a planar view of an antenna and/or a conductive pattern formed according to the preferred application example of this invention.

Figure 6 is a cross sectional view along the 6-6 line of Figure 5, further describing the antenna device according to a preferred example of this invention.

Figure 7 is a cross sectional view similar to Figure 6, describing the antenna device according to another preferred example of this invention.

Figure 8 is a cross sectional view similar to Figure 6, describing the antenna device according to another preferred example of this invention.

Figure 9 is a cross sectional view similar to Figure 2, describing the antenna device according to another preferred example of this invention.

Figure 10 is a cross sectional view similar to Figure 6, describing the antenna device according to another preferred example of this invention.

Figure 11 is a cross sectional view similar to Figure 2, describing the antenna device according to yet another preferred example of this invention.

According to the preferred examples of this invention, the radio frequency identification tags use printed antenna formed on a substrate. The said substrate may form a portion of an article, a package, a package container, a certificate, a freight bill, a label and/or an identification badge. In the preferred application example of this invention, printing is use to deposit ink, forming conductive pattern on a

substrate; coupling area is formed in the printed pattern, then coupling area is precisely formed in the conductive pattern of the corresponding substrate.

Referring to Figure 1 which is showing an exploded assembly view of a radio frequency identification tag 14 that includes a radio frequency identification circuit chip ("circuit chip") 12, secured to an antenna 10. The antenna may be forming the basis for a portion of a personal identification badge, a certificate, a freight bill, a tag, a package container (such as a box, or an envelop), or forming part of them. As can be understood, antenna 10 may also be forming the basis for a radio frequency identification tag circuit chip assembly (i.e., substrate and conductive pattern), such as described in an above mentioned US patent, entitled "Radio frequency identification tag with an article integrated antenna) that is not departing from the scope of this invention. As can be seen, the antenna 10 includes a conductive pattern 22 arranged on the substrate 16.

Continuing to refer to Figure 1, substrate 16 may be paper, plastic (including polyester or moralized polyester material), synthetic paper, reinforced paper, card (-board), synthetic paper coated card (-board) and selected products for special applications. Substrate 16 includes a first surface 18 and a second surface 20. Forming on the first surface 18 is a conductive pattern 22 that is including a first antenna element 24 and a second antenna element 26. Each of the first antenna element 24 and the second antenna element 26 is a conductive material bonded to or formed on the substrate 16. Most preferably, each of the first antenna 24 and the second antenna 26 is formed by printing using a proper printable conductive medium. For example, when printing on paper and/or card (-board), carbon/graphite base inks may be used to form an effective pattern 22. Synthetic or coated papers may also be used; however, the cost is higher. For printing on plastic materials, especially, silver or other precious metal inks may be used; however, such selection is rather limited due to a higher material cost. The conductive pattern 22 shown is in a H shape, it is suitable for electrostatic application. It should be understood that other printable patterns that are more suitable for inductive coupling, are within the scope of this invention. The first coupling area 28 is used to form the first antenna element 24, and the second coupling area 30 is used to form the second antenna element 26. The first coupling area 28 and the second coupling area are usually extending towards a slit 31 at center of the H shaped pattern formed on the substrate 16; they are separated by the said slit.

Referring to Figures 1 and 2, conductive soldering pad 38 and conductive soldering pad 40, designed to couple to conductive pattern 22, are formed on circuit chip 12. As shown in the figures, the conductive soldering pad 38 and conductive soldering pad 40 are "raised" ("bumped") soldering pads. Namely, they are protruded outward from the bottom surface 32 of the circuit chip 12. This is opposite to "surface" soldering pads; surface soldering pads are basically formed in the common plane with the bottom surface of 32 of the circuit chip. When secured to antenna 10, the conductive soldering pad 38 is connected to the first coupling area 28, while conductive soldering pad 40 is connected to the second coupling area 30. As shown in Figure 2, a conductive adhesive layer 34, and a conductive adhesive layer 36 are set up, between conductive solder pad 38 and the first coupling area 28, conductive solder pad 40 and the second coupling area 30, respectively, providing electrical connection and bonding the circuit chip

12 to the antenna 10. In a preferred application example of this invention, an isotropic adhesive is used and is precisely applied to either one of the circuit chip or the antenna 10. In another fashion, anisotropic adhesive may also be used, but it is more expensive. It should also be noted that there is no preference in using the bumped soldering pad; but bumped soldering pad surface (flat) soldering pad or recessed soldering pad (i.e., the formed soldering pad is recessed into the outer surface of the circuit chip 12) may all be used; its selection is based on cost and specific application. In the read/write application example, the circuit chip 12 may be conveniently prepared by using a TEMIC e5550 (available from TEMIC North America Inc., Basking Ridge, N. J.) chip. In the read only application example, an Indala 1341 circuit chip may be used (available from Motorola Indala Corp., San Jose, California).

A preferred anisotropic adhesive may be a 3M 9703 adhesive available from 3M Co., Ltd. The preferred adhesive is anisotropic, in which it only conducts electricity in the Z or vertical direction (Figure 2). The said adhesive is prepared from an adhesive base containing small metal coated micro spheres, allowing the adhesive layer to have electrical contact from the upper surface to the bottom surface. While in the X and Y directions, namely, in the plane of the adhesive layer, it is not forming electrical contact. Therefore, adhesive may be applied over the entire layer without shorting out the adjacent conductor lines. A preferred isotropic adhesive is No. 8103, available from Adhesives Research, Inc..

To be conducive to the understanding of this invention, refer to Figure 3; which is showing an antenna 10' in an intermediate processing stage. Antenna 10' is representing antenna 10 in an intermediate processing stage. For distinction, "primed" reference numbers are used to identify incompletely formed elements that are in their intermediate processing stage. Referring to Figure 3, even use a very accurate printing process, conductive pattern 22' will have distortion (deformation) in the X and Y directions with respect to edges 42 and 44 of the substrate 16', respectively. Usually, the deformations are expressed as $\pm x$ and $\pm y$, and is approximately in the order of 0.5 mm in each direction. In addition, referring to Figure 4, peripheral 45 of conductive pattern 22' is not a sharp line, which is the result of non-uniform drying, causing the peripheral 46 (? Only 45 is shown in Figure 3) to have a rough profile, a line with "bleeding" from the conductive ink. The peripheral 46 (? 45) deformation in Figure 4 is expressed as $\pm e$, which can reach as high as ± 0.125 mm. The total deformation resulting from both the position variation and bleeding can range as high as ± 1.5 mm. The significance of this number is that because the circuit chip 12 is only 1 mm square. Therefore, the deformation in the conductive pattern may be larger than the circuit chip 12 itself. As a result, it is impossible to position the circuit 12 to the conductive pattern 22 using only edge 42 and edge 44 as references. Therefore, automatic attachment of the circuit chip 12 requires complicated and expensive imaging processing in order to place conductive pattern accurately on the substrate 16. Another option to the expensive image processing is manual attachment. Manual attachment is time consuming and is unable to provide the repeatability of automated processing. Under either condition, cost, quality, and process efficiency are greatly impacted.

Referring to Figure 5, antenna 10 is in a completed stage which is including forming a slit 31 on substrate 16, separating the first coupling area 28 and the second coupling area 30. According to a preferred application example of this invention, slit 31 is formed by punching out a portion of substrate 16, at the center of the conductive pattern 22 relative to a substrate reference.

Referring to Figures 5 and 6, antenna 10' is positioned inside a fixture 100. Fixture 100 includes a corner locator block 102 and an edge locator block 104 extending above base 106. Another approach for positioning design may be using a pin locking hole/slot locator formed on the base substrate 16. The corner locator block 102 is arranged to engage both edge 42 and edge 44, and is using edge 42 and edge 44 to provide a substrate reference. The edge locator block 104 is arranged to engage edge 44. Using this approach, opposing edge 42 and edge 44 are used to establish a consistent and repeatable reference for slit 31. As shown in Figure 6, a punch (head) 108 is also secured relative to the fixture 100. During operation, antenna 10' is positioned with respect to the corner locator block 102 and the edge locator block 104 on the substrate 16. When punch 108 punches through the conductive pattern 22' and substrate 16' and entering buttonhole slit 120, punch 108 engages the conductive pattern 22' and the substrate 16', and punching out a plug 112. Thus, the slit 31 is accurately separating the first coupling area 28 and the second coupling area 30. In addition, the first coupling area 28 and the second coupling area 30 are accurately positioned with respect to edge 42 and edge 44, making simplified automated circuit chip 12 attachment possible. It can be expected that edge 46 of the first coupling area 28 and edge 48 of the second coupling area 30 are formed within ± 0.025 mm range from the edge 42 and the edge 44, respectively.

When completing the radio frequency identification tag 14, according to a preferred application example of this invention, the circuit chip element pick-and-place automated operation (not shown) may be arranged to reference edge 42 and edge 44. Base on the said reference, circuit chip 12 may be accurately positioned with respect to the first coupling area 28 and the second coupling area 30. It should be further understood that a single manufacturing/assembly unit may be constructed. Such assembly unit provides automated placement of substrate 16', prints conductive pattern 22' by using proper print head, forming slit 31, as well as positioning circuit chip 12. However, according to the preferred application examples of this invention, each of these operations may be accomplished by an independent manufacturing/assembly unit; for example, accomplished in a production line fashion. Throughout the entire process, accurate formation of the first coupling area 28 and the second coupling area 30 with respect to substrate 16, as well as accurate placement of circuit chip 12 with respect to these areas, are being maintained. This invention is advantageously providing distinctive manufacturing flexibility.

Referring to Figure 7 which is showing another form of preferred application example of this invention. An antenna 10' again representing the antenna 10 in its intermediate stage of processing. For distinction, "primed" reference numbers are used to identify incompletely formed elements that are in their intermediate processing stage (as shown in Figure 3). As can be seen from Figure 7, punch 208 is arranged to cut out (portion of) conductive circuit 22' and surface 18, and is pressing against substrate 16', but not punching out a through hole in substrate 16'. Fixture 100 is constructed as described above, and is including a corner locating block 102 and an edge locating block 104. The button hole slit 120 is omitted. The punch 208 is pressed against the conductive pattern 22' and surface 18' at the demarcation line separating the first coupling area 28' and the second coupling area 30'. Punch 208 is further

punching out a portion of the substrate 16' to create a notch 231 that is segregating the first coupling area 28 and the second coupling area 30. Again, obtain very accurate positioning of the first coupling area 28 and the second coupling area 30 with respect to the edge 42 and the edge 44; thus allowing automated placement of circuit chip 12. In Figure 8, punch 308 is designed to have a cutter edge 330, in order to better penetrate the conductive pattern 22' and surface 18, thus forming the notch 331 on the substrate 16.

Referring to Figure 9, when completing the radio frequency identification tag 114 according to a preferred application example of this invention, the pick-and-place automated operation (not shown) for the circuit chip may be arranged to reference the edge 42 and the edge 44. Based on the said reference, the circuit chip 12 may be positioned accurately by using an adhesive 34 to connect conductive soldering pad 38 to the first coupling area 28, and using an adhesive 36 to connect conductive soldering pad 40 to the second coupling area 30. The first coupling area 28 and the second coupling area 30 are accurately positioned and electrically insulated through notch 231 which is penetrating conductive pattern 22 and surface 18 and into substrate 16.

Figure 10 is representing another preferred application example of this invention, in which an antenna 110 is formed from the antenna 10'. Antenna 10' is still representing the antenna 110 in an intermediate processing stage. For distinction, "primed" reference numbers are used to identify incompletely formed elements that are in their intermediate processing stage (as shown in Figure 3). Fixture 400 includes a corner locator block 402 and an edge locator block (not shown), extending above base 406. Another approach for positioning design may be using a pin locking hole/slot locator formed on the base substrate 16'. The corner locator block 402 is arranged to engage both edges (shown as edge 142 in Figure 10) of substrate 116; the edge locator block is designed to engage an edge of substrate 116 as described. Forming/punch 408 is secured relative to the fixture 400 (? Only fixture 200 is shown in Figure 10). Punch 408 is also include a punch head portion 410, which is designed to engage the conductive pattern 22' and the substrate 16' and shear off a plug 412 when it is penetrating through the conductive pattern 22' and the substrate 16' and into the button hole slit 420. In this manner, it is forming slit 431 in the substrate 16', segregating the coupling area 128 and the coupling area 130. In addition, the first coupling area 128 and the second coupling area are precisely located with respect to the substrate 116, making it possible to simplify automated attachment of circuit chip 112.

Punch 408 may be further designed to have a shoulder or forming portion 424. When the punch 408 is engaging substrate 16', local area 418 of the substrate 16' is being compressed and is forming a shape basically corresponding to shoulder 424. In this manner, it is forming an indented groove 416 near the slit 431 in the substrate 116; the first coupling area 128 and the second coupling area 130 are extending into the indented groove 130.

Referring to Figure 11, a radio frequency identification 414 is assembled using an antenna 110. According to a preferred application example of this invention, the circuit chip element pick-and-place automated operation (not shown) may be arranged to reference an edge (edge 142 as shown in Figure 11) of the substrate 116. Based on the said reference, the circuit chip 112 may be positioned accurately by

using an adhesive 134 to connect conductive soldering pad 138 to the first coupling area 128, and by using an adhesive 136 to connect conductive soldering pad 140 to the second coupling area 130. The first coupling area 128 and the second coupling area 130 are accurately positioned and segregated through slit 431 which is penetrating the conductive pattern 122 and the substrate 116. In this manner, the circuit 112 is coupled to each of the first antenna element 124 and the second antenna element 126 arranged on the surface 118 of the substrate 116. In addition, the circuit chip 112 is maintained below the surface 118, thus reduce the chance of substrate to move during the application of the radio frequency identification tag 414. It should also be understood that filler material and/or cap may be placed on top of the circuit chip 112, thus providing further protection.

All in all, referring to Figure 1 again, the radio frequency identification tag 14 includes a radio frequency identification tag circuit chip 12, secured to an antenna 10. The said antenna includes a first antenna element 24 and a second antenna element 26 forming on the surface 18 of the substrate 16. The first antenna element and the second antenna element are separated and precisely positioned by a slit 31 formed in the substrate.

Referring to Figure 7 and Figure 8, another preferred application example of the antenna 10 includes forming a first antenna element 24 and a second antenna element 26 on surface 18 of a substrate 16. The first antenna element and the second antenna are accurately positioned and segregated through notches 231 and 331, which are penetrating through the said surface and partially extended into substrate, as described in Figure 7 and Figure 8.

Referring to Figure 9, a radio frequency identification 214, includes a radio frequency identification tag circuit chip 12, is secured to an antenna 10. The antenna includes a first antenna element 24 and a second antenna element 26 forming on the surface 18 of the substrate 16; and the first antenna element and the second antenna element are separated and precisely positioned by a notch 31 formed in the substrate.

In yet another preferred application example of this invention, referring to Figure 10, antenna 110 is including formation of a first antenna element 124 and a second antenna element 126 on surface 118 of substrate 116. The said substrate includes an indented groove 416 formed on the substrate. A first antenna element includes a first coupling area 128, while a second antenna includes a second coupling area 130. The first coupling area and the second coupling area are extending into the indented groove, and are separated and precisely positioned by a slit 431 formed in the indented groove.

Referring to Figure 11, a radio frequency identification tag 414, includes a radio frequency identification tag circuit chip 112, is secured to an antenna 110. The said antenna includes a first antenna element 124 and a second antenna element 126 forming on the surface 118 of the substrate 116. Antenna 110 also includes an indented groove 416 formed on the substrate 116; and the first coupling area 128 and the second coupling area 130 are extending into the indented groove, and are separated and precisely positioned by a slit 431 formed in the indented groove. The radio frequency identification tag circuit

chip is secured in the indented groove, and is coupled to the first coupling area and the second coupling area. Through the first coupling area and the second coupling area, the radio frequency identification tag circuit chip is coupled to the first antenna element and the second antenna element.

According to a preferred method for preparing radio frequency identification tag, a substrate is provided with a surface. Conductive pattern is printed on the said surface, and a slit is formed on the said substrate with respect to a reference; the slit separate the conductive pattern into a first antenna element and a second antenna element. A radio frequency identification tag circuit chip is secured on the substrate and is connected to the first antenna element and the second antenna element. The method may also provide a notch and/or an indented groove on the substrate.

Now, certain advantages of this invention will be discussed here:

The limitations on controlling printed antenna dimension and position tolerance have prevented the cost effective and performance enhancing technology from being used in a radio frequency identification tag. This invention has overcome these tolerance limitations enable the use printed antenna technology.

At the same time reducing the cost of the radio frequency identification tag, its performance is improved by using printed antenna with easily matched radio frequency identification tag circuit chip.

The manufacturing efficiency is improved through this invention, in which the radio frequency identification tag circuit chip is rapidly and precisely secured and coupled to the radio frequency identification tag antenna.

This invention allows a single unit or multiple units manufacturing approaches; using commonly used pick-and-place automated chip placement operation to manufacture radio frequency identification tag.

There are many other changes and modifications which are not departing from the scope and spirit of this invention. The above discussions touch upon some of the scope of changes. Other scope of changes will be apparent from the attached claims.

[19]中华人民共和国国家知识产权局

[51]Int. Cl⁷

G08B 13/14

[12] 发明专利申请公开说明书

[21] 申请号 99807676.7

[43]公开日 2001年9月26日

[11]公开号 CN 1315027A

[22]申请日 1999.6.18 [21]申请号 99807676.7

[30]优先权

[32]1998.6.23 [33]US [31]09/103,226

[86]国际申请 PCT/US99/13645 1999.6.18

[87]国际公布 WO99/67754 英 1999.12.29

[85]进入国家阶段日期 2000.12.21

[71]申请人 摩托罗拉公司

地址 美国伊利诺斯州

[72]发明人 诺埃尔·H·埃伯哈特

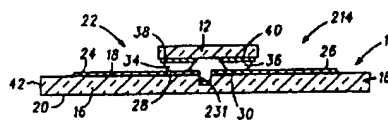
[74]专利代理机构 中原信达知识产权代理有限责任公司
代理人 余 朦 李 辉

权利要求书 2 页 说明书 11 页 附图页数 3 页

[54]发明名称 具有印刷天线的射频识别标签和方法

[57]摘要

一种射频识别标签(14)包括一射频识别标签电路芯片(12),射频识别标签电路芯片耦合到包括印刷在基片(16)上的导电图形(22)的天线(10)。该基片可以形成物品、包装、包装容器、信封、证件、运货单、标签和/或认证徽章之一的一部分。该导电图形包括第一耦合区(28)和第二耦合区(30),被设计成耦合到射频识别标签电路芯片上。第一耦合区和第二耦合区通过形成在该基片上的缝隙(31)精确定位并且相互隔离。



I S S N 1 0 0 8 - 4 2 7 4

权 利 要 求 书

1. 一种射频识别标签，包括：

5 一射频识别标签电路芯片，固定到天线上，该天线包括形成在基片表面上的第一天线单元和第二天线单元，第一天线单元和第二天线单元通过形成在基片上的缝隙隔离开。

10 2. 权利要求 1 的射频识别标签，第一天线单元包括第一耦合区而第二天线单元包括第二耦合区，并且该缝隙将第一耦合区和第二耦合区隔离开。

3. 权利要求 2 的射频识别标签，第一耦合区和第二耦合区被设计成与射频识别标签电路芯片耦合。

15 4. 权利要求 1 的射频识别标签，该缝隙相对基片基准形成。

5. 权利要求 1 的射频识别标签，该天线是印刷在基片表面上的导电图形。

20 6. 权利要求 1 的射频识别标签，一种导电黏合剂将射频识别标签电路芯片耦合到该天线上。

7. 一种用于射频识别标签的天线，包括：

25 一印刷在基片表面上的导电图形，和一形成在基片上的缝隙，将导电图形隔离成为第一天线单元和第二天线单元。

8. 权利要求 7 的天线，第一天线单元包括第一耦合区而第二天线单元包括第二耦合区，第一耦合区和第二耦合区由缝隙限定。

30 9. 权利要求 7 的天线，该天线形成物品、包装、包装容器、信

封、证件、运货单、标签和认证证章之一的一部分。

10. 权利要求 7 的天线，该缝隙相对基片基准形成。

5 11. 一种制造射频识别标签的方法，该方法包括以下各步骤：

提供具有表面的基片；

在该表面上印刷导电图形；

在该基片上相对基片基准形成缝隙，该缝隙将导电图形隔离成为
第一天线单元和第二天线单元；和

10 将射频识别标签电路芯片电连接到第一天线单元和第二天线单
元。

15 12. 权利要求 11 的方法，其中印刷导电图形的步骤包括印刷由
第一耦合区和第二耦合区连接的第一天线单元和第二天线单元，并且
形成缝隙的步骤，包括形成将第一耦合区和第二耦合区隔离开的缝
隙。

说明书

具有印刷天线的射频识别标签和方法

5 本申请是 Noel H. Eberhardt 等人于 1998 年 6 月 9 日提交的申请
序号为_____的“具有物品集成天线的射频识别标签”，代理记录
号 IND10149 的共同转让的美国专利申请的后续部分申请，该在先申
请在此引用作为参考，如同在此将这些公开内容一字不差地进行阐述
所具有相同效果。

10 本申请与下列共同转让的在先美国专利申请有关。Ted Geiszler
等人于 1995 年 10 月 11 日提交的申请序号为 08/540813 的“远端供电
电子标签和相关激励器/读取器和有关方法”，代理记录号 IND00701；
Victor Allen Vega 等人于 1998 年 2 月 27 日提交的申请序号为 09/031848
15 的“利用为耦合接地设计的标签的射频识别标签系统”，代理记录号
IND10153；Victor Allen Vega 等人于 1998 年 3 月 12 日提交的申请序
号为 09/041480 的“为磁存储标签状态信息设计的射频识别标签”，
代理记录号 IND10146；以及 Victor Allen Vega 等人于 1998 年 3 月 20
日提交的申请序号为 09/045357 的“具有可编程电路状态的射频识别
20 标签”，代理记录号 IND10174；这些在先申请在此引用作为参考，
如同在此将这些公开内容一字不差地进行阐述所具有相同效果。

 本发明总的涉及射频识别标签领域，包括但不限于具有印刷天线
的射频识别标签。

25 射频识别标签和射频识别标签系统是公知的，并且有许多应用。
例如，射频识别标签经常用于自动门卫应用中的人员认证，以保护固
定的建筑或地区的安全。在射频识别标签中存储的信息识别寻求进入
被固定建筑的人。射频识别标签系统方便地提供在短距离内利用射频
30 (RF) 数据传输技术从射频识别标签中读取信息。通常，用户简单地

手持或将射频识别标签放在接近基站处，该基站向包含在射频识别标签中的射频识别标签的供电电路发射激励信号。该电路响应于激励信号，将存储的信息从射频识别标签传送给基站，由基站接收和解码该信息。通常，射频识别标签能够保持和在工作中发射丰富的信息——

5 足够用于唯一识别个人，包装，库存等的信息。

供电和读取射频识别标签的典型技术是电感耦合或电感电源耦合和电容数据耦合的组合。电感耦合利用射频识别标签中的线圈元件。该线圈元件被来自基站的激励信号所激励，为射频识别标签电路提供

10 电源。射频识别标签线圈，或第二线圈，可以用于在射频识别标签和基站之间发射和接收所存储的信息。依赖电感耦合的射频识别标签对射频识别标签相对基站的方向敏感，因为由激励信号产生的电场必须与线圈元件以基本上直角相交才能有限耦合。电感耦合装置的读取范围一般在几个厘米数量级。对于某些应用，例如电子宠物识别、行李跟踪、包裹跟踪和库存管理应用需要更长的读取距离。

15

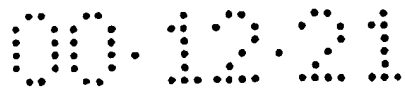
对射频识别标签供电和读取的另一个技术是静电耦合，例如在上述参考应用中所公开的射频识别标签系统和射频识别标签中所采用的。这些系统有利地提供了对于现有技术的那些应用明显增加的读/写

20 距离。从所公开的系统和标签的使用获得的另一个优点是用户不需要将射频识别标签靠近基站或对着基站方向。因此，有可能将基站的天线合并到例如门口或门厅、包裹传送机或物品分类系统中，以在更大距离上对标签供电和读取标签信息。

为在基站和射频识别标签之间耦合电感或静电信号，标签必须包括一个具有至少一个，通常为两个的天线单元的天线。通常，标签电路芯片和天线电连接并粘合到标签基片上。由标签基片尺寸所决定的标签尺寸一般保持非常小。因此，天线通常受尺寸限制。可是，更小的天线不利地影响了读取范围。天线也必须与标签基片形成在同平面上，这潜在地使标签对方向敏感。因为不希望，通常也不现实，将射

25

30



频识别标签制造得更大，有效的天线尺寸仍然受限制。通常平面的标签设计也限制了天线是平面的、方向敏感的构形。

按照标题为“具有物品集成天线的射频识别标签”的上述美国专利
5 申请所公开发明的优选实施例，建议把天线集成到物品上。例如，
优选实施例利用把导电墨水印刷在卡片或纸包装上的天线。然后将射
频识别标签电路芯片固定在物品上并且与该天线电连接。另外，建议
提供射频识别标签芯片组件。该芯片组件提供将射频识别标签电路芯
10 片粘合在包括导电图形的基片上。如同所公开的，通过利用导电墨水
将图形印刷在纸基片上来形成优选导电图形。然后可将该芯片组件固
定在物品上并且通过导电图形与该天线电连接。

如同所理解的，电路芯片与印刷在物品上天线或与印刷在基片上
导电图形的对准对于该电路芯片正常工作是非常重要的。更具体地，
15 电路芯片必须定位在大约 ± 0.125 毫米（mm）内，以将电路芯片上的
导电焊盘与该天线和/或导电图形正确配合。可是，在纸或纸类材料上
印刷天线和/或导电图形的的一般技术只获得在 $\pm 1.5\text{mm}$ 数量级的边
缘公差。此边缘公差的大小大于一般的电路芯片。产生不严密边缘公
差的几个因素包括印刷图形边缘渗漏和印刷图形相对基片位置改变。

20 因此，需要一种改善的射频识别标签。

在附图中将说明本发明优选示范性实施例，图中相同的参考标号
代表相同的部件。

25 图 1 是按照本发明优选实施例的射频识别标签的分解装配图。

图 2 是图 1 沿线 2-2 的截面图。

图 3 是天线和/或导电图形印刷在基片上的平面图。

图 4 是图 3 中在圆圈 A 中天线部分的放大平面图。

图 5 是图 4 中按照本发明优选实施例形成的天线和/或导电图形
30 平面图。



图 6 是图 5 中沿线 6-6 的截面图，进一步说明按照本发明的一个优选实施例制作天线的装置。

图 7 是类似图 6 的截面图，说明按照本发明的另一个优选实施例。

图 8 是类似图 6 的截面图，说明按照本发明的另一个优选实施例。

5 图 9 是类似图 2 的截面图，说明按照本发明的另一个优选实施例。

图 10 是类似图 6 的截面图，说明按照本发明的另一个优选实施例。

图 11 是类似图 2 的截面图，说明按照本发明的另一个优选实施例。

10

按照本发明优选实施例的射频识别标签利用了形成在基片上的印刷天线。该基片可以形成物品、一个包装、一个包装容器，一个证件，一个货运单、一个标签和/或一个认证证章的一部分。在本发明的优选实施例中，通过印刷沉积墨水，在基片上形成导电图形，在印刷图形中形成耦合区，然后在导电图形中相对基片精确地形成耦合区。

15

20

参照图 1，在分解装配图中所示的射频识别标签 14 包括一个射频识别标签电路芯片（“电路芯片”）12，固定在天线 10 上。天线 10 可以形成个人认证证章、证件、货运单、标签、包装容器（例如盒子或信封）一部分的基础，或形成它们的一部分。如同可以理解的，天线 10 也可以形成射频识别标签电路芯片组件的基础（即基片和导电图形），如同在题目为“具有物品集成天线的射频识别标签”的上述美国专利申请中所描述的，而并不脱离本发明的范围。如同所见，天线 10 包括安置在基片 16 上的一个导电图形 22。

25

30

继续参照图 1，基片 16 可以是纸、塑料（包括聚酯和金属化的聚酯材料）、合成纸、强化纸，卡片、合成纸涂层卡片和为特定应用所选择的物品。基片 16 包括第一表面 18 和第二表面 20。形成在第一表面 18 上的导电图形 22 包括第一天线单元 24 和第二天线单元 26。第一天线单元 24 和第二天线单元 26 的每个由粘合或形成在基片 16

上的导电材料形成。最好，第一天线单元 24 和第二天线单元 26 的每个利用适合的可印刷的导电介质通过印刷形成。例如，当印刷在纸和/或卡片上时，碳/石墨基墨水形成有效导电图形 22。另外可使用合成和涂层纸，但增加成本。特别为在塑料上进行印刷，可以使用银和其它贵金属墨水，但由于材料成本较高而较少选择。所示的导电图形 22 具有 H 形状，适合于用在静电应用中。应当理解，可以印刷更适合于例如电感耦合的其它图形而不脱离本发明范围。用第一耦合区 28 形成第一天线单元 24 和用第二耦合区 30 形成第二天线单元 26。第一耦合区 28 和第二耦合区 30 向着形成在基片 16 上通常在 H 形状中心的缝隙 31 延伸并由该缝隙隔离。

参照图 1 和图 2，由为耦合到导电图形 22 而设计的导电焊盘 38 和导电焊盘 40 形成电路芯片 12。如图所示，导电焊盘 38 和导电焊盘 40 是“凸起”焊盘。即，它们从电路芯片 12 的底表面 32 向外突出。这与“表面”焊盘相反，表面焊盘基本上形成在与电路芯片底表面 32 的共平面上。当固定在天线 10 上时，导电焊盘 38 电连接到第一耦合区 28 而导电焊盘 40 电连接到第二耦合区 30。如图 2 所示，导电黏合剂层 34 和导电黏合剂层 36 分别安置在导电焊盘 38 与第一耦合区 28 之间和导电焊盘 40 与第二耦合区 30 之间，提供电连接并将电路芯片 12 粘合到天线 10 上。在本发明的优选实施例中，各向同性黏合剂被使用并且精确施加在电路芯片 12 和天线 10 之一或两者上。另一个方式，各向异性黏合剂也可以使用但成本高。也应当注意，并没有使用凸起焊盘的特别爱好，也可以使用凸起焊盘、表面焊盘或凹槽焊盘（即，所形成的导电焊盘凹进在电路芯片 12 的外表面内），其根据成本和特定应用而选择。在读/写实施例中，电路芯片 12 可以由 TEMIC e5550 电路芯片（可以从 TEMIC NORTH AMERICA 公司，Basking Ridge, New Jersey 获得）方便地构成。在只读实施例中可以使用 Indala1341 电路芯片（可以从 MOTOROLA INDALA 公司，San Jose, California 获得）。

5 优选的各向异性黏合剂是可以从 3M 公司获得的 3M 9703 黏合剂。优选黏合剂是各向异性的，其中它只在 Z 或垂直方向导电（图 2）。该黏合剂制造得在黏合剂基底中包含镀金属的微小颗粒，使黏合剂层从上表面到下表面形成电接触。而在 X 或 Y 方向，即黏合剂层的平面上没有形成电接触。因此，黏合剂可以施加在整个层而不短路相邻导线。优选的各向同性黏合剂是#8103 可以从 ADHESIVES RESEARCH 公司获得。

10 为有助于理解本发明，参照图 3，示出天线 10'处在中间处理阶段。天线 10'代表天线 10 的中间制造阶段。为清楚，最初的参考标号用于识别在中间阶段没有完全形成的元件。参照图 3，天线 10'通过首先在基片 16'上最好是印刷形成导电图形 22'。如同可以看到的，缝隙 31 还没有形成，而第一耦合区 28'和第二耦合区 30'在导电图形 22'的中心仍是相连的。

15 图 3 也说明了与在基片 16'上形成导电图形 22'有关的制造公差。这些公差和它们对完成的天线 10 的影响的讨论将提供对本发明优点更多的理解。参照图 3，即使利用非常精确的印刷工艺，导电图形 22'将分别在相对基片 16'的边缘 42 和边缘 44 的方向 X 和 Y 上变形。通常变形分别表示为 $\pm X$ 和 $\pm Y$ ，在每个方向为大约 0.5mm 数量级。另外，参照图 4，导电图形 22'的周边 45 不是明显的线，由不均匀干燥的结果，致使周边 46 具有粗糙的轮廓，而代之以导电墨水的“渗漏”。周边 46 的变形在图 4 中表示为 \pm ，可以大到 $\pm 0.125\text{mm}$ 。由图形位置变化和渗漏两者产生的总变形可以高达 $\pm 1.5\text{mm}$ 范围。此数字的重要性是因为电路芯片 12 只是 1mm 见方。因此，导电图形的变形可能大于电路芯片 12。结果，仅参照边缘 42 和边缘 44 将电路芯片 12 定位到导电图形 22 上是不可能的。因此自动附着电路芯片 12 需要复杂、
25 昂贵的图象技术，以将导电图形 22 精确地放置在基片 16 上。对昂贵图象自动处理的另一个选择是人工附着。人工附着耗费时间并且不能
30 提供自动处理的工艺重复性。在任何一个情况下，成本、质量和加工

效率受很大影响。

5 参照图 5，完成阶段的天线 10 包括形成在基片 16 上的缝隙 31，将第一耦合区 28 和第二耦合区 30 隔离。按照本发明的优选实施例，缝隙 31 通过在相对基片基准的导电图形 22 的中心冲压掉基片 16 一部分形成。

10 参照图 5 和图 6，天线 10' 定位在夹具 100 中。夹具 100 包括角定位块 102 和边缘定位块 104，延伸在基座 106 上。另一个方式的定位设计可以使用形成在基片 16 上的针啮合孔/缝定位器。角定位块 102 安排成与边缘 42 和边缘 44 两者啮合，利用边缘 42 和边缘 44 提供基片基准。边缘定位块 104 安排成与边缘 44 啮合。以此方式，相对边缘 42 和边缘 44 建立了形成缝隙 31 的一致的、可重复的基准。图 6 所示，一个冲头 108 还被相对夹具 100 固定。在工作中，天线 10' 相对基板 106 上的角定位块 102 和边缘定位块 104 定位。当冲头 108 穿过导电图形 22' 和基片 16' 并且进入扣眼缝隙 120 时，冲头 108 啮合导电图形 22' 和基片 16' 从中剪切下塞子 112。这样缝隙 31 精确地将第一耦合区 28 和第二耦合区 30 隔离。另外，第一耦合区 28 和第二耦合区 30 相对边缘 42 和边缘 44 精确定位，有可能简化电路芯片 12 的自动附着。可以预计，第一耦合区 28 的边缘 46 和第二耦合区的边缘 48，
15 20 可以分别形成距边缘 42 和边缘 44 在 $\pm 0.025\text{mm}$ 的范围内。

25 在完成按照本发明优选实施例的射频识别标签 14 时，电路芯片的元件拾取-放置自动操作(未图示)可以对基准边缘 42 和边缘 44 进行安排。根据该基准，电路芯片 12 可以相对第一耦合区 28 和第二耦合区 30 精确定位。应当进一步理解，可以构成单一的制造/组装元件。这种组装元件提供自动安置基片 16'，利用适合的打印头印刷导电图形 22'，形成缝隙 31，并定位电路芯片 12。可是，按照本发明的优选实施例，这些操作的每个可以按单独制造/组装元件的安排来完成，例如以生产线的形式来完成。在整个过程中，保持相对基片 16 精确形
30

成第一耦合区 28 和第二耦合区 30 并且相对这些区域精确安置电路芯片 12。这样，本发明有利地提供了制造的明显灵活性。

参照图 7，表示本发明另一个方式的优选实施例。天线 10'再次代表天线 10 的中间制造阶段。为清楚，最初的参考标号用于表示在中间阶段没有完全形成的元件（如图 3 所示）。如图 7 所见，冲头 208 安排得切断导电图形 22'和表面 18 并且挤压基片 16'一部分而不形成基片 16'中的通孔。夹具 100 按上述构成，并且包括角定位块 102 和边缘定位块 104。省略了扣眼缝隙 120。冲头 208 在第一耦合区 28'和第二耦合区 30'分界线上啮合导电图形 22'和表面 18'，在啮合点处切断导电图形 22'和表面 18。冲头 208 进一步挤压基片 16'的一部分，以致产生隔离第一耦合区 28 和第二耦合区 30 的缺口 231。再次获得第一耦合区 28 和第二耦合区 30 相对边缘 42 和边缘 44 非常精确的定位，由此允许自动安置电路芯片 12。在图 8 中，冲头 308 被设计成具有刀刃边缘 330，以更好地刺入导电图形 22'和表面 18，而形成基片 16 上的缺口 331。

然后参照图 9，在完成按照本发明优选实施例的射频识别标签 114 时，电路芯片元件拾取-放置自动操作（未示出）可以对基片 16 的基准边缘 42 和边缘 44 进行安排（图 9 所示边缘 42）。根据该基准，电路芯片 12 可以利用通过黏合剂 34 将导电焊盘 38 电连接到第一耦合区 28 和通过黏合剂 36 将导电焊盘 40 电连接到第二耦合区 30 而精确定位。第一耦合区 28 和第二耦合区 30 通过穿过导电图形 22 和表面 18 进入基片 16 的缺口 231 精确定位并且电绝缘。

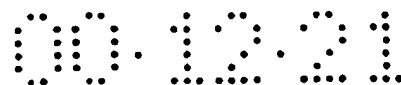
图 10 表示本发明另一个优选实施例，用于从天线 10'形成天线 110。天线 10'仍代表天线 110 的中间制造阶段，和为清楚，最初的参考标号用于表示在中间阶段没有完全形成的元件（如图 3 所示）。夹具 400 包括角定位块 402 和边缘定位块（未示出）延伸到基底 406 上。另一个方式的定位设计可以使用形成在基片 16'上的针啮合孔/缝定位

器。角定位块 402 被安排成啮合基片 116 的两个边缘（在图 10 所示边缘 142），边缘定位块按所描述的被设计成啮合基片 116 的一个边缘。成型/冲头 408 还被相对夹具 400 固定。冲头 408 包括一个冲头部分 410，被设计成当它穿过导电图形 22'和基片 16'并且进入扣眼缝隙 420 时，啮合导电图形 22'和基片 16'从中剪切下塞子 412。以此方式，在基片 16'上形成缝隙 431 将耦合区 128 和耦合区 130 隔离。另外，第一耦合区 128 和第二耦合区 130 相对基片 116 精确定位，有可能简化电路芯片 112 的自动附着。

冲头 408 进一步被设计成具有肩部或成型部分 424。当冲头 408 啮合基片 16'时，基片 16'的局部区域 418 被压缩并且形成基本上对应肩部 424 的形状。以此方式，在基片 116 上缝隙 431 附近形成凹槽 416，第一耦合区 128 和第二耦合区 130 延伸到凹槽内。

参照图 11，使用天线 110 组装射频识别标签 414。按照本发明的优选实施例，电路芯片元件拾取-放置自动操作（未示出）可以被安排成参照基片 116 的边缘（图 11 中所示的边缘 142）。根据该基准，电路芯片 112 可以利用通过黏合剂 134 将导电焊盘 138 电连接到第一耦合区 128、通过黏合剂 136 将导电焊盘 140 电连接到第二耦合区 130 而精确定位。第一耦合区 128 和第二耦合区 130 精确地定位并且通过延伸穿过导电图形 122 和基片 116 的缝隙 431 相互隔离开。以此方式，电路芯片 112 耦合到安置在基片 116 表面 118 上的第一天线单元 124 和第二天线单元 126 的每个上。另外，电路芯片 112 保持在表面 118 之下，由此减少的使用射频识别标签 414 期间从基片 116 移动的可能性。也应当理解，填充材料和/或盖子可以安置在电路芯片 112 上方，由此提供进一步保护。

总之，再次参照图 1，射频识别标签 14 包括一个射频识别标签电路芯片 12，固定在天线 10 上。该天线包括形成在基片 16 的表面 18 上的第一天线单元 24 和第二天线单元 26。第一天线单元和第二天线



单元被形成在基片内的缝隙 31 隔离和精确定位。

参照图 7 和图 8，天线 10 的另一种方式的优选实施例包括形成在基片 16 的表面 18 上的第一天线单元 24 和第二天线单元 26。第一天线单元和第二天线单元由形成穿过该表面和部分延伸到基片内分别表示在图 7 和图 8 的缺口 231 和 331 隔离和定位。

参照图 9，射频识别标签 214 包括一个射频识别标签电路芯片 12，固定在天线 10 上。该天线包括形成在基片 16 的表面 18 上的第一天线单元 24 和第二天线单元 26，而第一天线单元和第二天线单元由形成在基片内的缺口 31 隔离并精确定位。

在本发明的又一个优选实施例中，参照图 10，天线 110 包括形成在基片 116 的表面 118 上的第一天线单元 124 和第二天线单元 126。该基片被形成为包括形成在该基片上的凹槽 416。第一天线单元包括第一耦合区 128 而第二天线单元包括第二耦合区 130。第一耦合区和第二耦合区延伸到凹槽内并且由形成在凹槽内的缝隙 431 隔离和精确定位。

参照图 11，射频识别标签 414 包括射频识别标签电路芯片 112，固定在天线 110 上。该天线包括形成在基片 116 的表面 118 上的第一天线单元 124 和第二天线单元 126。天线 110 还包括形成在基片 116 内的凹槽 416，并且第一耦合区 128 和第二耦合区 130 延伸到凹槽内并且由形成在凹槽内的缝隙 431 隔离和精确定位。射频识别标签电路芯片固定在凹槽内并且耦合到第一耦合区和第二耦合区。第一耦合区和第二耦合区由此将射频识别标签电路芯片耦合到第一天线单元和第二天线单元。

按照制造分配认证标签的优选方法，提供一具有表面的基片。在该表面上印刷导电图形，和在该基片上相对基片基准形成缝隙，该缝

隙将导电图形隔离成为第一天线单元和第二天线单元。然后射频识别标签电路芯片被固定在基片上并且与第一天线单元和第二天线单元电连接。该方法可以另一种方式提供在基片上形成缺口和/或凹槽。

5 现在讨论本发明的某些优点。

控制印刷天线尺寸和定位公差能力方面的极限已经限制了在射频识别标签方面的该项成本有益和强化性能的技术。本发明通过克服这些公差极限有助于利用印刷天线技术。

10

在减少射频识别标签成本的同时，通过利用容易匹配射频识别标签电路芯片的印刷天线改进了性能。

15

通过本发明改善了制造效率，其中射频识别标签电路芯片被迅速和精确地固定并且耦合到射频识别标签天线上。

本发明也允许用单一元件和多个元件制作方案，利用普通可用的元件拾取-放置自动操作经济地制造射频识别标签。

20

可以进行许多另外改变和修改而不脱离本发明范围和精神。上面讨论的某些改变的范围。其它修改的范围根据附带的权利要求书是显而易见的。

说 明 书 附 图

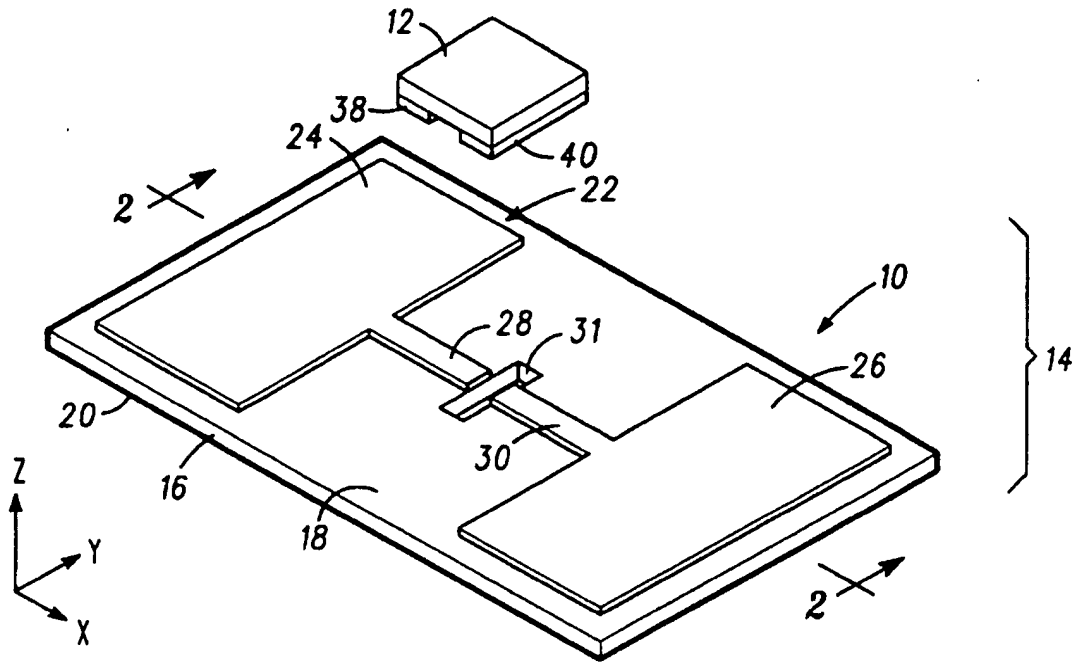


图1

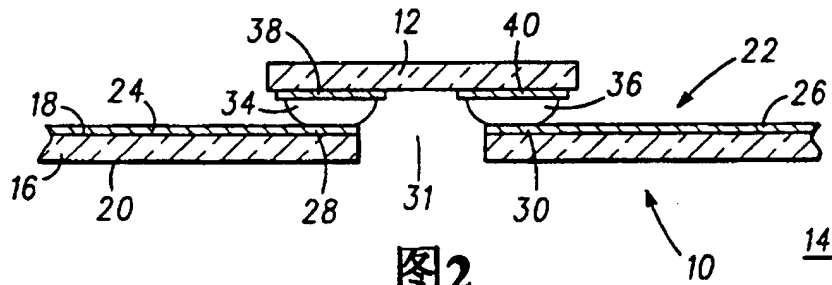
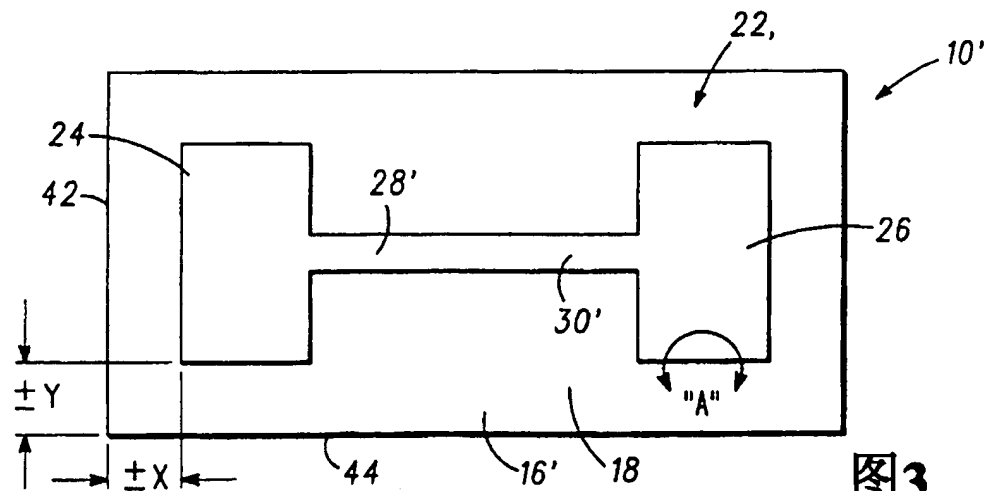


图2



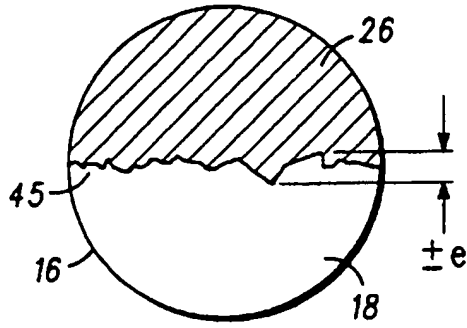


图4

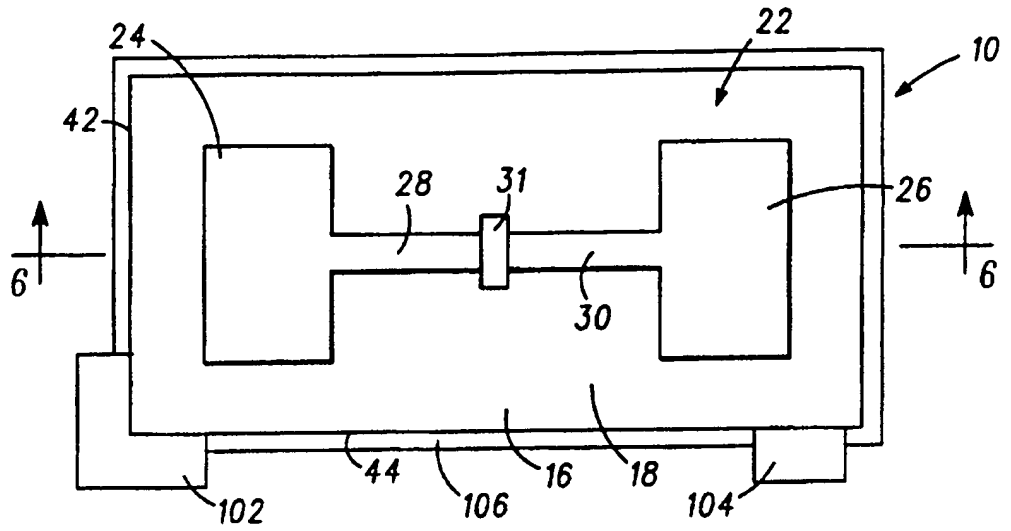


图5

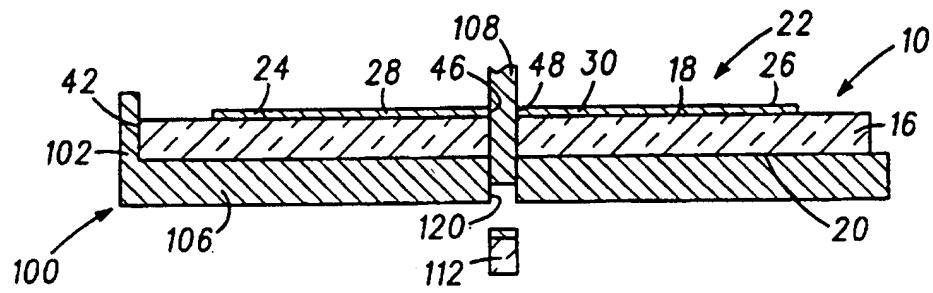


图6

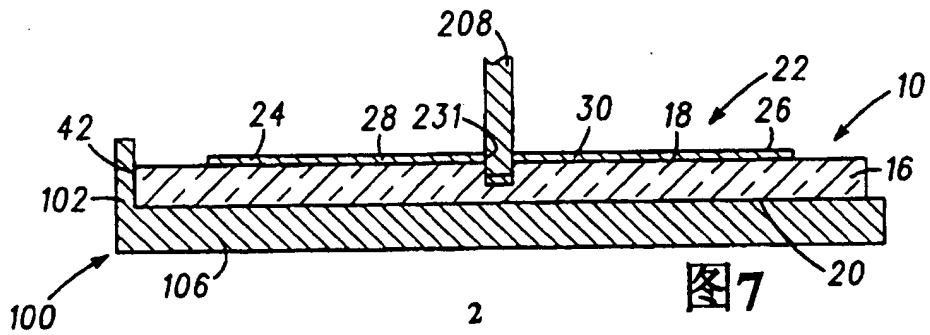


图7

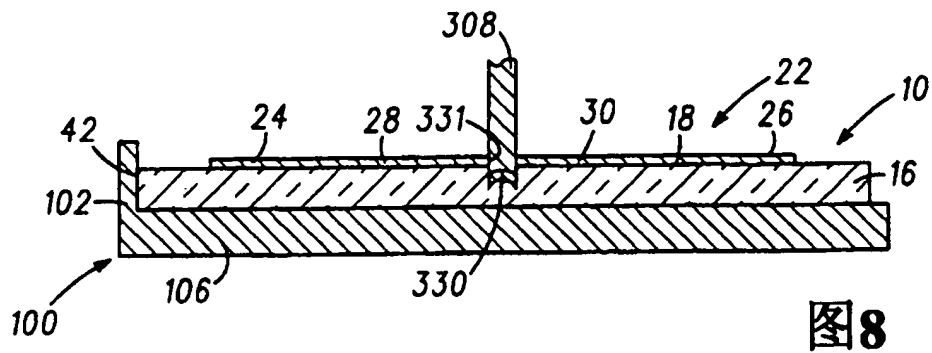


图8

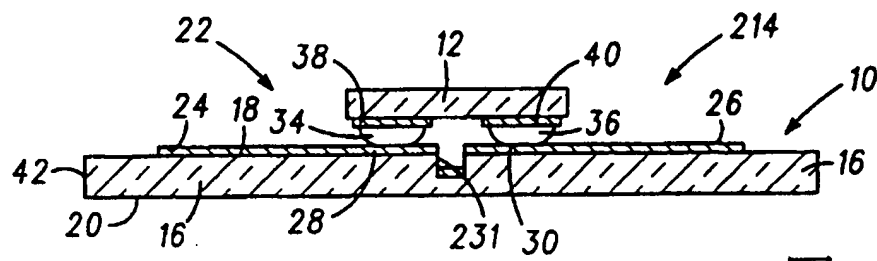


图9

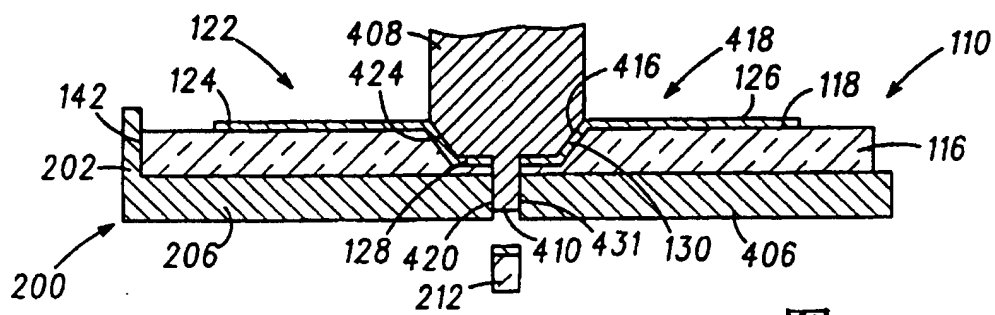


图10

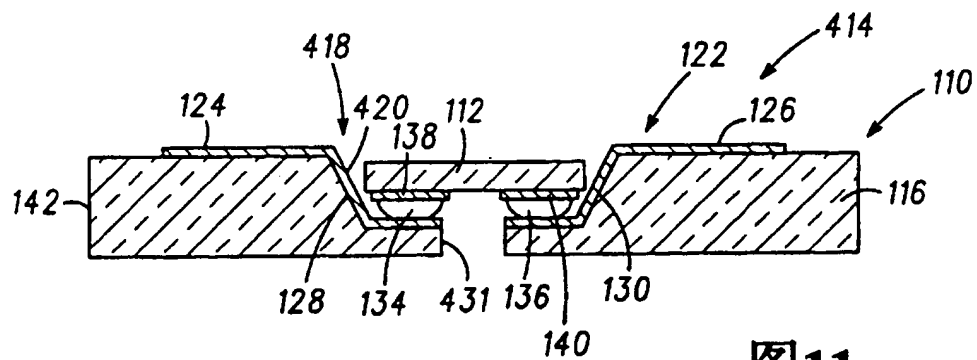


图11

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☒ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.